Application of New PLL in Active Atomic Frequency Standard Circuit

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Abstract—**Based on the research of the group phase relationship between two signals with different frequencies, a new PLL by directly phase comparing and locking between two signals with different frequencies (the paper following will call this new PLL DPCLDF-PLL）. The application of DPCLDF-PLL on the circuit design of active atomic frequency standards, can simplify the circuit, and obtain higher performance as well.**

I. INTRODUCTION

Active atomic frequency standards can be seen as a complex PLL. Because of the complex relationship between the frequency of microwave signal caused by the atomic energy level transition and the VCOCXO signal, it is necessary to do some frequency transformation, such as frequency multiplying, mixing and synthesizing , to get the normalized frequency. In every transformation segment, it will bring some additional noise, which will influence the short term stability and phase noise performance of the output signal. In this paper, by replacing the traditional PLL with the DPCLDF-PLL, the complex frequency transformation circuit can be gotten rid of, and the additional noise brought by the circuit would be decreased.

II. THE PRINCIPLE OF DPCLDF-PLL

A. Group phase relationship and pulse sample technique

The phase relationship between two periodical signals, f_A and f_B, changes periodically in their group period T_{group}. A group period contains several minimum common multiple period T_{minc}'s. Supposed that $f_A = Af_{maxc}$, $f_B = Bf_{maxc}$, where A and B are two prime positive integers, and f_{maxc} is the maximum common factor frequency, its period $T_{minc}=1/f_{maxc}$ is called the minimum common multiple period [4].

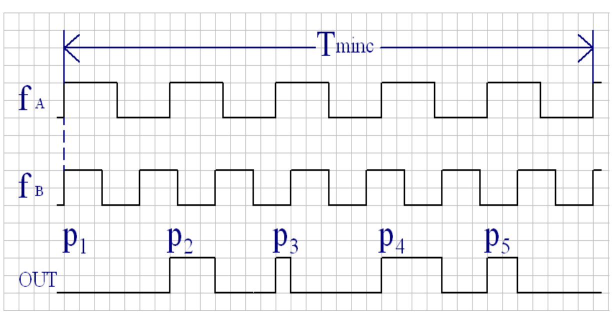

Figure 1. Group phase coincidence

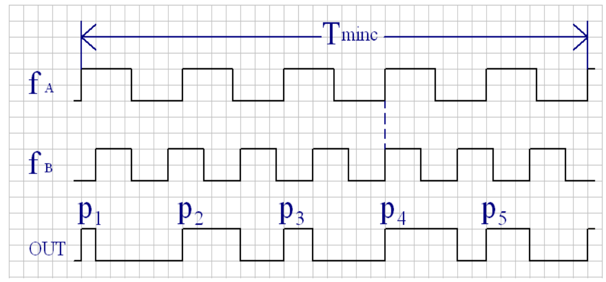

Figure 2. Next group phase coincidence after A T_{group}'s

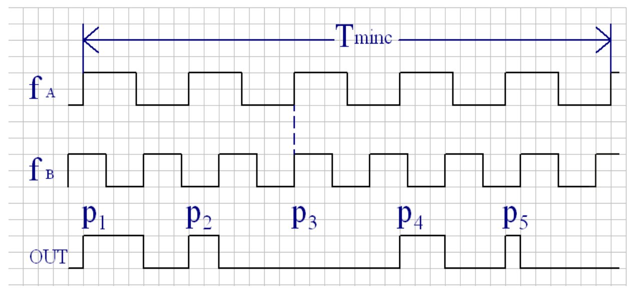

Figure 3. Broadening of the width of P1

Fig.1 shows the situation of group phase coincidence of f_A and f_B. Because tiny phase shift exists between f_A and f_B, supposed that the phase of f_B delays slowly, after n T_{minc}'s, the group phase coincides again, as shown in Fig.2. And then it is believed that the group period of f_A and f_B is that T_{group}=n* T_{minc}. Obviously the value of T_{group} depends on the rates of phase shift of f_A and f_B.

The waveform "OUT", shown in Fig.1 and Fig.2, is the output waveform of Sequential PD with f_A and f_B as its inputs, of which the rising edges of f_A set the output, and the rising edges of f_B clear the output. If the moment the group phase coincidence occurs is taken as the start , and in the each following T_{minc}, let the signal "OUT" pass through "Pulse sampling", and only allow a special pulse to output, here we take the first pulse P_1 for example. With the phase shift of the two signals, the width of P_1 becomes larger and larger. Fig.3 shows the group phase relationship and the output situation of the Pulse Sampling after (A-1) group period T_{group}. Therefore, take the situation of Fig.1 as the start, the width of P_1 is becoming from zero to the largest slowly, and after A T_{group} it

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returns to the situation, so the variation period of the width of P_1 is A* T_{group}.

B. The Principle of DPCLDF-PLL

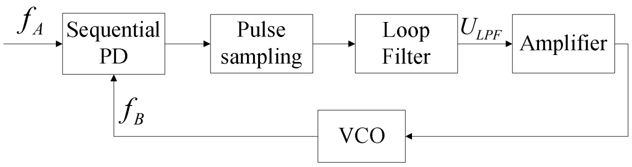

Figure 4. Block diagram of DPCLDF-PLL

Fig.4 shows the principle block diagram of DPCLDF-PLL, the reference signal f_A and the output signal f_B are put into sequential PD directly, of which the rising edges of f_A set the output, and the rising edges of f_B clear the output. Through the Pulse Sampling, a special pulse of the PD output in each T_{minc} is picked out, and it passes through a low-pass filter, and it is amplified properly to control the VCO, then high precision locking will be realized.

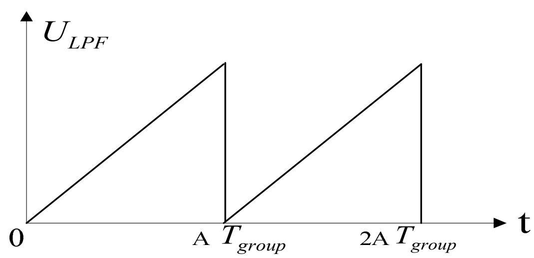

Figure 5. The output voltage waveform of low-pass filter in unlock state

Fig.5 shows the output voltage of low-pass filter, U_{LPF}, in unlock state, which changes periodically in A T_{group}'s. At this time, the Equivalent Phase Comparison Frequency of f_A and f_B is f_B, and the phase processing resolution is B times the traditional frequency normalizing technique. Therefore DPCLDF-PLL is simple in circuit and higher in locking precision.

III. APPLICATION OF DPCLDF-PLL IN ACTIVE HYDROGEN ATOM FREQUENCY STANDARD CIRCUIT

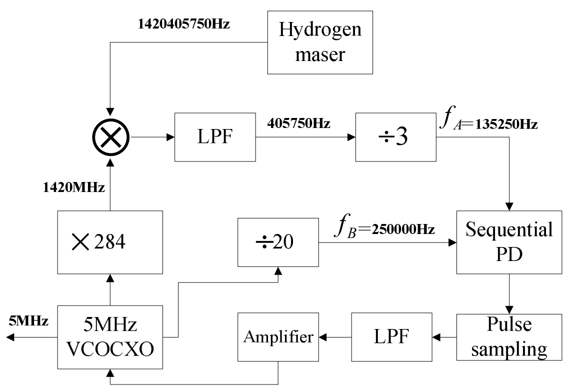

Figure 6. New principle diagram of active Hydrogen atomic frequency standard

Fig.6 is the new principle diagram of active Hydrogen atomic frequency standard improvement, a 1420405750Hz signal generated by Hydrogen maser is mixed with 1420MHz signal which multiplied by 5MHz VCOCXO signal, and the output is passed through a low pass filter, then a difference frequency signal will be obtained and be frequency divided, here frequency division coefficient is 3, then the signal f_A of 135250Hz which equals to 250*541 is obtained; the 5MHz signal generated by VCOCXO is frequency divided by the frequency division coefficient of 20, then the signal f_B of 250000Hz which equals to 250*1000 will be gotten. So, here A=541, B=1000, f_{maxc}=250Hz. f_A and f_B are sent to a sequential phase detector, where the rising edges of f_A will set the output of phase detector, and the rising edges of f_B will clear the output of phase detector, then the output of phase detector is sent to a pulse sampler and low pass filter, and then it is amplified to control the VCOCXO. Equivalent Phase Comparison Frequency f_{equ} is 875MHz which equals to f_B*1420405750/405750. This Equivalent Phase Comparison Frequency can meet the high resolution of phase processing and be realized simply in circuit. The device only needs one mixer and simple frequency division circuit, and the noise will be reduced greatly.

IV. APPLICATION EXPERIMENTS OF DPCLDF-PLL

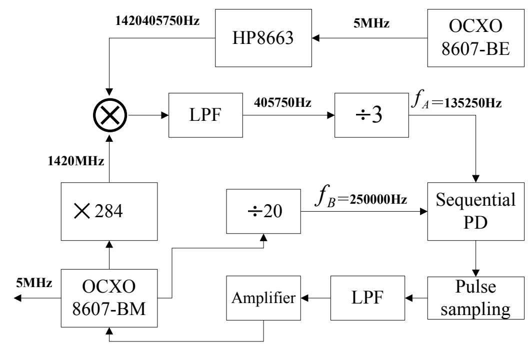

Figure 7. Experiment diagram of DPCLDF-PLL

Fig.7 is the experiment diagram of DPCLDF-PLL circuit, for convenient, here we use OCXO8607-BE and HP8663 to generate a 1420405750Hz signal instead of Hydrogen maser, and take this signal as the reference of DPCLDF-PLL to lock OCXO8607-BM. Where the output of the OCXO8607-BE is a stable 5MHz signal and OCXO8607-BM is voltage controllable.

TABLE I. STABILITY OF OCXO8607-BM AFTER LOCKED

$\tau = 0.1S$	$\tau = 1S$	$\tau = 10S$
$3.9\times10^{-13}/\tau$	$2.1\times10^{-13}/\tau$	$1.5\times10^{-13}/\tau$

TABLE II. SSB OF OCXO8607-BM AFTER LOCKED

1Hz	10Hz	100Hz
-110dBc	-125dBc	-140dBc

Tab.1 is the short-term stability of OCXO8607-BM after locked, and Tab.2 is its single sideband phase noise. The stability and phase noise performance of the OCXO8607-BM output signal are both very high. From experiments data, we can see that the additional noise of the DPCLDF-PLL is very low. If the circuit is improved further and the circuit noise will be reduced, then better short-term stability and better phase noise will be obtained.

Ⅴ. CONCLUSION

DPCLDF-PLL shows many advantages such as simple circuit and low additional noise, so it is of great use in the improvement of atomic frequency standard circuit, and the potential of physical package can be excavated too, then the short-term stability, phase noise of the atomic frequency standard will be improved.

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